STRUCTURE AND METHOD FOR A JUNCTION FIELD EFFECT TRANSISTOR WITH REDUCED GATE CAPACITANCE

ABSTRACT OF THE INVENTION

An apparatus and method for a semiconductor device with reduced gate capacitance. Specifically, an n-channel or p-channel junction field effect transistor (JFET) is described comprising an appropriately doped substrate forming a drain region, an epitaxial layer formed on top of the substrate, a control structure comprising a gate region implanted into the epitaxial layer, a source region sharing a p-n junction with the gate region, and an altered epitaxial region. The altered epitaxial region is formed by implanting either n^- or p^- dopants directly below the gate region of either the n-channel or p-channel JFET for widening a depletion region surrounding the gate region. The enlarged depletion region reduces the gate capacitance of the JFET between the gate and drain regions.